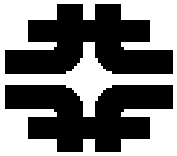


Fermilab

Particle Physics/Electrical Engineering Department

Specification for the CMS HCAL Readout Box Backplane

Theresa Shaw
October 16, 2002

Backplane Introduction

This specification will describe the backplane functions of the readout boxes used for CMS Hadron Barrel (HB), Hadron Endcap (HE) and Hadron Outer (HO) Calorimeter front end electronics.

Due to mechanical constraints, the Readout Boxes (RBX) for each of the three detector areas (HB, HE and HO) have a different mechanical design. Because of this, the HB, HE and HO backplanes are also forced to have a unique shape.

Backplane Functions

Low Voltage Distribution

2 Backplane Voltages

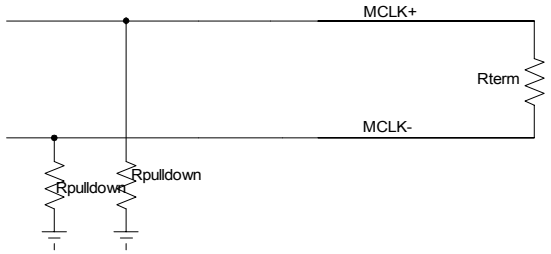
V1 (minimum of 2 Universal Power Module Connectors for V1)
(6.5V regulated to 5V)
V2 (minimum of 2 Universal Power Module Connectors for V2)
(4.5V regulated to 3.3V and 2.5V)
GND (minimum of 4 Universal Power Module Connectors for GND)

Connectors allow for power sequencing

Bulk Capacitors (Ceramic) distributed on backplane (located on backside)

Master Clock Distribution

The Master Clock will be driven as a differential LVPECL signal from the Clock and Control Module (CCM) module. No more than three loads will be driven by any individual clock line. Termination of the differential signal will be accomplished with a backplane resistor between the differential pair at the load end. Pulldown resistors will be located at the source. Controlled impedance routing will be done on all clock signals.



In the case of the HB backplane, 5 separate clock lines will be driven to 5 defined groupings on the backplane.

No attempt will be made to used matched length routing between the different groupings.

RBXbus Serial Interface

The backplane must support the RBXbus serial interface. This is similar in protocol to I^2C. The RBXbus serial interface is a 2 wire interface. It consists of a clock line and an open drain data line.

Like the Master Clock, the serial interface is broken into groupings of three or less module slots.

The serial clock is distributed and terminated just like the Master Clock signal.

The data line is an open drain line. Each line will have a load of up to 15 devices (3 modules x (3 Channel Control ASICs + 2 Serializers)).

To help in the serial bus addressing, each readout card slot will use two pins to encode a geographical slot number. This allows us to supply 2 of the 7 RBXbus address bits directly from the backplane. The other bits will be hardwired on the readout cards.

Backplane geographical pins are either grounded or left floating. The lines will have weak pull-up resistors on the readout modules, which will turn the floating pins into logic highs.

Beam Zero Marker

The Beam Zero signal is driven out to the backplane as LVPECL by the CCM. Two separate copies of the Beam Zero signal will be driven out. In the case of the HB backplane, one copy of the signal is driven to the right of the CCM, and one copy to the left of the CCM. The maximum number of loads on the line will be 9. The line is terminated on the backplane.

Reset

The Reset signal is driven out to the backplane as LVPECL by the CCM. Two separate copies of the Reset signal will be driven out. In the case of the HB backplane, one copy of the signal is driven to the right of the CCM, and one copy to the left of the CCM. The maximum number of loads on the line will be 9. The line is terminated on the backplane.

Reset_PLL

The Reset_PLL signal is driven out to the backplane as LVPECL by the CCM. Two separate copies of the Reset_PLL signal will be driven out. In the case of the HB backplane, one copy of the signal is driven to the right of the CCM, and one copy to the left of the CCM. The maximum number of loads on the line will be 9. The line is terminated on the backplane.

TEMP

One readout card in each grouping of two or three module returns the output of a temperature transducer which will be used to determine the temperature of its area in the Readout box.

Reset_PWR

A single ended LVTTL line which will reset the voltage section of the Front End modules following an over current trip.

PWR_Trip

A wired-or line which will signal that a FE module has had an over current trip.

Backplane Pin Assignments

READOUT Card Slot

Pin Number	Row A	Row B	Row C
1	GND	GND	GND
2	V1	V1	V1
3	GND	GND	GND
4	V2	V2	V2
5	GND	GND	GND
6	V2	V2	V2
7	GND	GND	GND
8	MCLK+	GND	SERCLK+
9	MCLK-	GND	SERCLK-
10		GND	SER_DAT
11	TEMP	GND	RESET_PLL+
12		GND	RESET_PLL-
13	GEO_ADDR(0)	GND	RESET+
14	GEO_ADDR(1)	GND	RESET-
15	BZERO+	GND	Reset_PWR
16	BZERO-	GND	PWR_Trip

CCM Module - TIMING Card

Pin Number	Row A	Row B	Row C
1	GND	GND	GND
2	V1	V1	V1
3	GND	GND	GND
4	V2	V2	V2
5	GND	GND	GND
6	V2	V2	V2
7	GND	GND	GND
8	MCLK3+	GND	MCLK6+
9	MCLK3-	GND	MCLK6-
10	MCLK2+	GND	MCLK5+
11	MCLK2-	GND	MCLK5-
12	MCLK1+	GND	MCLK4+
13	MCLK1-	GND	MCLK4-
14		GND	
15	BZERO1+	GND	BZERO2+
16	BZERO1-	GND	BZERO2-

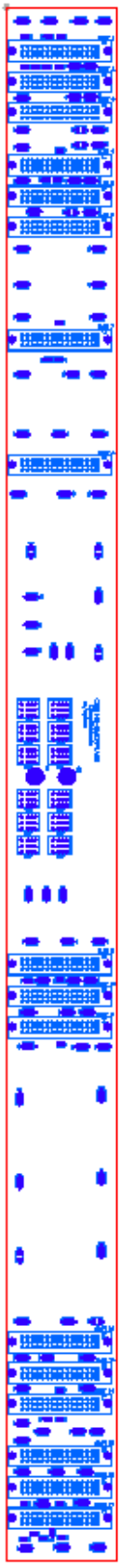
CCM Module – Serial Interface Driver

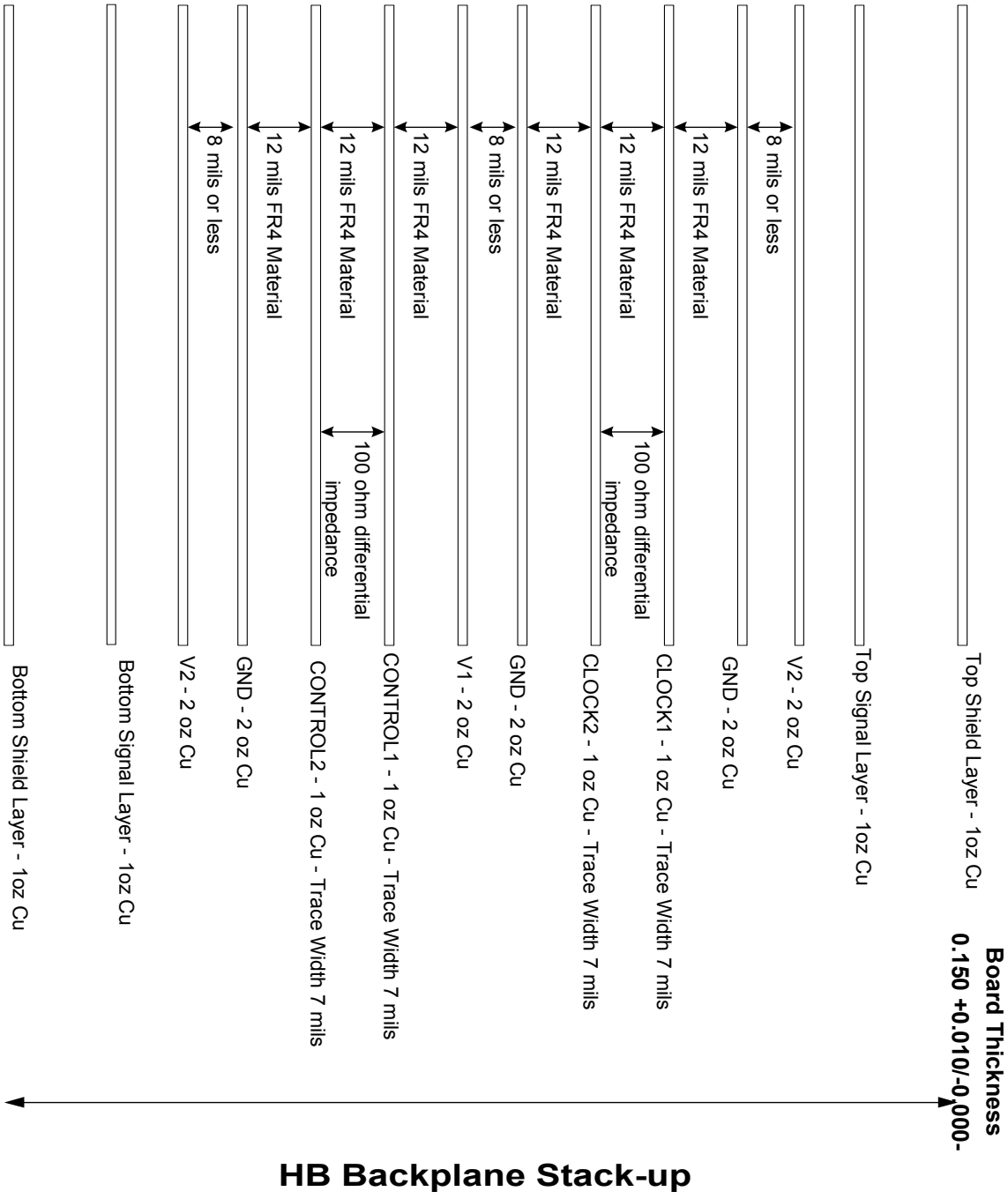
Pin Number	Row A	Row B	Row C
1	GND	GND	GND
2	V1	V1	V1
3	GND	GND	GND
4	V2	V2	V2
5	GND	GND	GND
6	V2	V2	V2
7	GND	GND	GND
8	SER_CLK3+	GND	SER_CLK6+
9	SER_CLK3-	GND	SER_CLK6-
10	SER_CLK2+	GND	SER_CLK5+
11	SER_CLK2-	GND	SER_CLK5-
12	SER_CLK1+	GND	SER_CLK4+
13	SER_CLK1-	GND	SER_CLK4-
14	SER_DAT3	GND	SER_DAT6
15	SER_DAT2	GND	SER_DAT5
16	SER_DAT1	GND	SER_DAT4

CCM Module – Temperature

Pin Number	Row A	Row B	Row C
1	GND	GND	GND
2	V1	V1	V1
3	GND	GND	GND
4	V2	V2	V2
5	GND	GND	GND
6	V2	V2	V2
7	GND	GND	GND
8	TEMP3	GND	TEMP6
9	TEMP2	GND	TEMP5
10	TEMP1	GND	TEMP4
11	RESET_PLL1+	GND	RESET_PLL2+
12	RESET_PLL1-	GND	RESET_PLL2-
13	RESET1+	GND	RESET2+
14	RESET1-	GND	RESET2-
15	Reset_PWR1	GND	Reset_PWR2
16	PWR_Trip1	GND	PWR_Trip2

HB Backplane





HB Backplane Stack-up